What is claimed is:

1. A semiconductor device having a metal silicide contact structure, comprising:

a substrate;

an insulation layer having an opening formed on the substrate;

a metal silicide layer formed in the opening of the insulation layer; and

a conductive layer formed on the metal silicide layer,

wherein the metal silicide layer is formed between the substrate and the conductive layer and the metal silicide layer has a thickness of less than about 100 Å.

2. A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer is a semiconductor layer.

3. A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the metal silicide layer is formed using a native metal silicide having a first phase and a second phase, the second phase having a first stoichiometrical composition ratio that is different from a second stoichiometrical composition ratio of the first phase.

4. A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the substrate is comprised of a material selected from the group consisting of silicon, silicon germanium, silicon-on-insulator (SOI), and silicon-germanium-on-insulator (SGOI).

5. A semiconductor device having a metal silicide contact structure as claimed in claim 1, further comprising a silicon layer or a silicon germanium layer in a form of a crystalline phase or an amorphous phase formed on the substrate.

6. A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer comprises a silicon layer or a silicon germanium layer in a form of a crystalline phase or an amorphous phase.

7. A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer is doped polycrystalline silicon.

8. A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the metal silicide layer has a resistance between about 3 to 20 Ω/□.

9. A semiconductor device having a metal silicide contact structure as claimed in claim 1, further comprising a gate oxide film formed on the substrate.

10. A semiconductor device having a metal silicide contact structure as claimed in claim 9, further comprising a gate stack formed on the gate oxide film.

11. A semiconductor device having a metal silicide contact structure as claimed in claim 10, further comprising gate sidewall spacers formed on the sides of the gate stack.

12. A semiconductor device having a metal silicide contact structure as claimed in claim 9, further comprising a source/drain area formed on the substrate exposed by the opening in the insulation layer.

13. A semiconductor device having a metal silicide contact structure as claimed in claim 1, further comprising:

field oxide films formed on the substrate; and

a pad layer formed between the field oxide films and below the metal silicide layer.

14. A semiconductor device having a metal silicide contact structure as claimed in claim 13, and further comprising:

a second insulation layer formed above the field oxide films and the pad layer;

a bit line stack formed on the second insulation layer; and

a third insulation layer formed on the bit line stack and the second insulation layer.

15. A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer is titanium nitride (TiN).

16. A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer is a metallic material.

17. A semiconductor device having a metal silicide contact structure as claimed in claim 15, further comprising a metal layer formed on the conductive layer.

18. A semiconductor device having a metal silicide contact structure, comprising:

a substrate;

a gate oxide film formed on the substrate;

a gate stack formed on the gate oxide film;

a metal silicide layer formed on the substrate and the gate stack; and

a capping layer formed above the metal silicide layer, wherein the metal silicide layer has a thickness less than about 100 Å.

19. A semiconductor device having a metal silicide contact structure as claimed in claim 18, further comprising:

a source/drain area formed on the substrate;

a lightly-doped source/drain area formed on the substrate between the metal silicide layer formed on the substrate and the gate oxide film; and

gate sidewall spacers formed on sides of the gate stack.

20. A method of forming a metal silicide layer in a semiconductor device comprising:

i) providing a substrate;

ii) forming an insulation layer on the substrate, the insulation layer having an opening therein;

iii) depositing a metal in the opening on the insulation layer so that a first layer including a native metal silicide layer of a first phase is formed at an interfacial surface between the substrate and the deposited metal;

iv) selectively removing the first layer while retaining the native metal silicide layer of the first phase;

v) forming a second layer made of a conductive material on the native metal silicide layer of the first phase and the insulation layer; and

vi) reacting the native metal silicide layer of the first phase with the substrate so as to transform the native metal silicide layer into a metal silicide layer having a second phase which has a first stoichiometrical composition ratio different from a second stoichiometrical composition ratio of the first phase and a thickness of less than about 100 Å.

21. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein the substrate comprises a material selected from the group consisting of: silicon, silicon germanium, silicon-on-insulator (SOI) and silicon-germanium-on-insulator (SGOI).

22. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, further comprising forming a silicon layer or a silicon germanium layer in a form of a crystalline phase or an amorphous phase on the substrate.

23. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein the second layer comprises a silicon layer or a silicon germanium layer in a form of a crystalline phase or an amorphous phase.

24. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein the second layer is comprised of a metal or a metallic material.

25. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein the second layer is a semiconductor layer.

26. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein the second layer is a doped polycrystalline silicon.

27. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein the second layer is comprised of titanium nitride (TiN).

28. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein the first layer is comprised of a material selected from the group consisting of cobalt (Co), titanium (Ti), tungsten (W), nickel (Ni), platinum (PT), hafnium (Hf), and palladium (Pd).

29. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein the first layer is deposited to a thickness of greater than about 50 Å.

30. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 20, wherein, in reacting the native metal silicide layer of the first phase, the native metal silicide layer of the first phase is transformed into the metal silicide layer of the second phase using a heat-treatment process.

31. A method of forming a metal silicide layer in a semiconductor device, comprising:

i) providing a substrate having formed thereon a gate oxide film, a gate stack having sides, the gate stack having gate sidewall spacers on the sides thereof;

ii) depositing a metal on the substrate, the gate stack and the gate sidewall spacer, the gate stack including a conductive material including a silicon, in such a manner that a first layer including a native metal silicide layer of a first phase is formed at an interfacial surface between the silicon and the deposited metal;

iii) selectively removing the first layer while retaining the native metal silicide layer of the first phase;

iv) depositing a first capping layer on a resulting structure; and

v) reacting the native metal silicide layer of the first phase with the silicon so as to transform the native metal silicide layer into a metal silicide layer having a second phase which has a first stoichiometrical composition ratio different from a second stoichiometrical composition ratio of the first phase, the metal silicide layer being formed to a thickness of less than about 100 Å.

32. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the substrate comprises a material selected from the group consisting of silicon, silicon germanium, silicon-on-insulator (SOI) and silicon-germanium-on-insulator (SGOI).

33. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the gate stack comprises a silicon layer or a silicon germanium layer in a form of a crystalline phase or an amorphous phase.

34. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the gate stack has a capping insulation layer at an upper surface thereof.

35. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the first capping layer comprises a metallic material.

36. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 35, wherein the first capping layer is comprised of a material selected from the group consisting of titanium nitride (TiN), titanium tungsten (TiW), tantalum nitride(TaN), and tungsten nitride (WN).

37. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the first capping layer is comprised of an insulation material.

38. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the first capping layer is comprised of a material selected from the group of SiN and SiON.

39. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the native metal silicide layer of the first phase is transformed into the metal silicide layer of the second phase using a heat-treatment process.

40. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, further comprising:

vi) removing the first capping layer; and

vii) depositing a second capping layer on a resulting structure.

41. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 40, wherein the second capping layer is made of an insulation material having an etching selectivity with respect to the metal silicide layer of the second phase.

42. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the first layer is comprised of a material selected from the group consisting of cobalt (Co), titanium (Ti), tungsten (W), nickel (Ni), platinum (Pt), hafnium (Hf) and palladium(Pd).

43. A method of forming a metal silicide layer in a semiconductor device as claimed in claim 31, wherein the first layer is deposited to a thickness of about 100 Å.